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# A new set of high speed matrix addressing schemes for ferroelectric liquid crystal displays

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# ERRATUM

## A new set of high speed matrix addressing schemes for ferroelectric liquid crystal displays

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Figures 2 and 4 of the above preliminary communication were inadvertently transposed and should have appeared as follows:

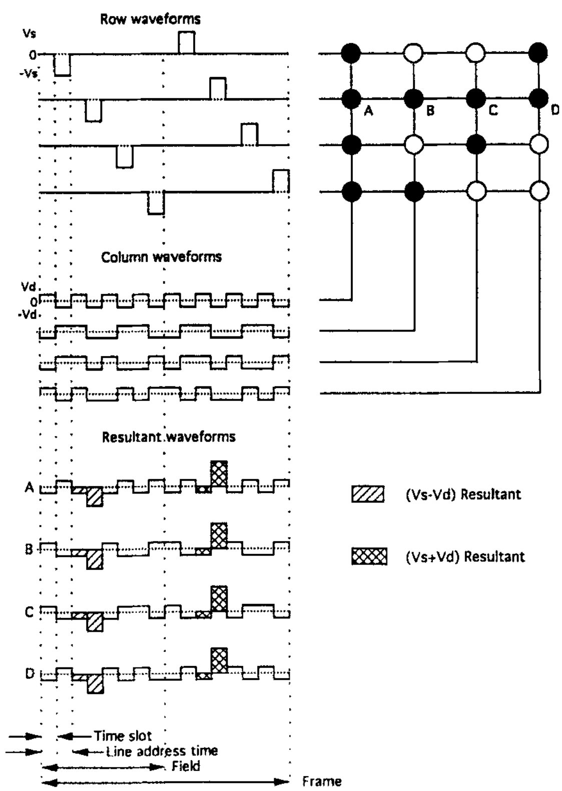


Figure 2. Simple example of the JOERS/Alvey drive scheme for the case of four way multiplexing. When operating in the $\tau$–$V$ minimum mode, the switch pulse will be $(V_s - V_d)$ and pulses of amplitude $(V_s + V_d)$ and $V_d$ will not switch. Pixel A is arbitrarily defined to be 'off' in response to a $-(V_s - V_d)$ pulse.

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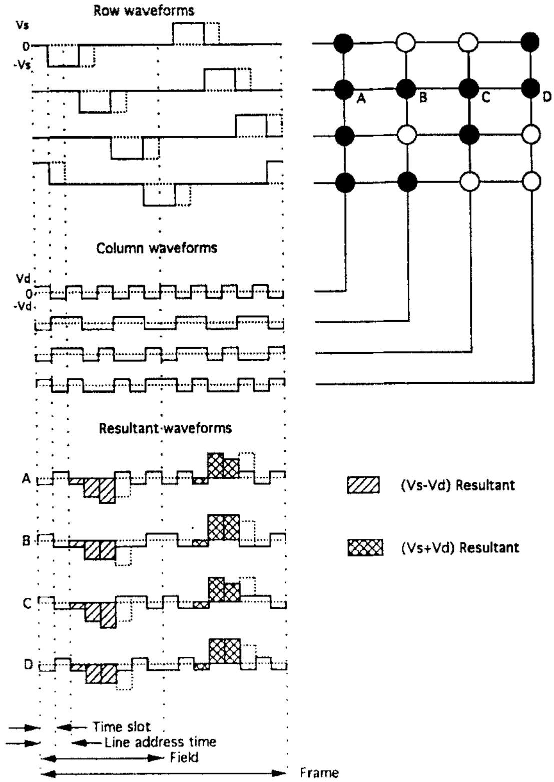


Figure 4. Simple example of the Malvern-2 (solid line) and Malvern-3 (dotted line) drive schemes for the case of four way multiplexing. When operating in the $\tau$–$V$minimum mode, the switching pulse will be ($V_s - V_d$) and pulses of amplitude ($V_s + V_d$) and $V_d$ will not switch. Pixel A is arbitrarily defined to be 'off' in response to a $-(V_s - V_d)$ resultant pulse.

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